REMARKS

Claims 1-15 are currently pending in the case. Claims 12-14 have been amended.

The applicant has studied the Office Action dated May 22, 2003 and has made the changes believed appropriate to place the application in condition for allowance. Reconsideration and reexamination are respectfully requested.

Applicant acknowledges with thanks the indication of allowance of Claims 2-11 and 15.

The title has been amended to recite "Semiconductor Devices Including Bi-Polar and Field Effect Transistors."

Applicant has submitted the attached replacement formal drawing sheet for Fig. 2, which was previously amended and approved by the Examiner.

Applicant has amended paragraph [0001] to insert the U.S. application number for the cited U.S. application.

Claims 12-14 have been amended to dependent form. Claims 12-14 each depend from claim 1.

Claims 1, 12, 13 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over WOLF "Silicon Processing for the VLSI Era" in view of Manning (6,137,146) and Schwank et al. (6,268,630). This rejection is respectfully traversed.

Claim 1 is directed to a semiconductor device comprising, *inter alia,* a field effect transistor and a bipolar transistor wherein "the first body region of the second conduction type is in contact with and thereby electrically connected to the first base region of the second conduction type ..." The Examiner has conceded that, in addition to other deficiencies, Wolf "does not disclose ... placing the first body region of the second conduction type in contact with and electrically connected to the first base region of the second conduction type ... ." In an attempt to overcome this deficiency of the Wolf reference, the Examiner has taken the position that it would be "obvious ... to place the first body region of the second conduction type of Wolf's semiconducting device in contact with and electrically connected to the first base region of the second conduction type such as taught by Manning, in order to save space on the surface of the semiconducting device to thus increase the density of the logic circuitry." The applicant strongly disagrees.

It is respectfully submitted that the references have been improperly combined and that the rejection of the claims based upon this improper combination should be withdrawn. The Examiner has cited no teaching, suggestion or recognition in the Manning reference of "sav[ing] space on the surface of the semiconducting device." On the contrary, the Examiner appears to be impermissibly using hindsight, that is, using the present applicants' disclosure to provide a motivation for combining the references, which motivation is wholly lacking from the Examiner's citations to the references. More specifically, the present applicant explicitly teaches:

> *Accordingly, by the manufacturing method in accordance with the present embodiment, the first p-type base region 220 can be electrically connected to the first p-type body region 50a without forming a contact layer for leading out the p-type base region 220.* Present specification, page 29, lines 13-16.

The Examiner has cited no teaching or suggestion in the Manning or Wolf references that a base region can be electrically connected to a body region to save surface space by not forming a contact layer for leading out the base region. Instead, the Examiner appears to be impermissibly engaged in using hindsight.

Moreover, it is noted that the bipolar device of Fig. 7-75(a) of the Wolf reference cited by the Examiner appears to be isolated from the FET device by a trench. Thus, it appears that to combine the references in the manner suggested by the Examiner, one of ordinary skill would need to ignore the explicit instructions of the Examiner's citation to the Wolf reference.

Still further, it is noted that in the device of the Examiner's citations to the Manning reference, the emitter region 36 and the source region 36 are the same region 36 as shown in Figs. 7 and 8 of the Manning reference. By contrast, claim 1 requires that "the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type ..." The Examiner has provided no explanation as to why one of ordinary skill would ignore that portion of the Manning reference which describes forming the emitter and the source from the same semiconductor region 36 yet be motivated by the descriptions of the base and body regions 26c of the Manning reference. The deficiencies of the Examiner's citations to the Wolf and Manning references are not met by the Examiner's citations to the Schwank reference.

Claims 12-14 now depend from claim 1 and are allowable for at least the reasons set forth above with respect to claim 1. It is therefore respectfully submitted that the references have been improperly combined and that the rejection of the claims based upon this improper combination should be withdrawn.

The Examiner has made various comments concerning the obviousness of certain features of the present inventions. Applicant respectfully disagrees. Also, the Examiner's comments are deemed moot in view of the above response.

In the statements of reasons for allowance of certain claims the Examiner provided various reasons for allowance. Applicant notes that the claims are directed to various combinations of features. It is respectfully submitted that the patentability of each of the allowed and allowable claims resides in the combination of features recited in that claim in addition to any features noted by the Examiner.

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is earnestly solicited.

Respectfully submitted,

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Alan S. Raynes

Alan S. Raynes Reg. No. 39,809 **Sept. 22, 2003 (Date)**